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Enhanced Environmental Stability Induced by Effective Polarization of a Polar Dielectric Layer in a Trilayer Dielectric System of Organic Field-Effect Transistors: A Quantitative Study

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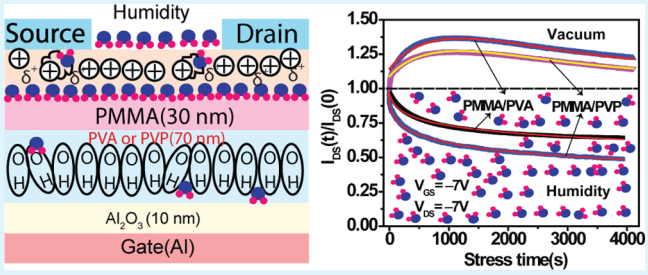
Supporting Information

ABSTRACT: We report a concept fabrication method that helps to improve the performance and stability of copper phthalocyanine (CuPc) based organic field-effect transistors (OFETs) in ambient. The devices were fabricated using a trilayer dielectric system that contains a bilayer polymer dielectrics consisting of a hydrophobic thin layer of poly-(methyl methacrylate) (PMMA) on poly(vinyl alcohol) (PVA) or poly(4-vinylphenol) (PVP) or polystyrene (PS) with Al_2O_3 as a third layer. We have explored the peculiarities in the device performance (i.e., superior performance under ambient humidity), which are caused due to the polarization of dipoles residing in the polar dielectric material. The anomalous behavior of the bias-stress measured under vacuum has been explained successfully by a stretched exponential function modified by adding a time dependent dipole polarization term. The OFET with a dielectric layer of PVA or PVP containing hydroxyl groups has shown enhanced characteristics and remains highly stable without any degradation even after 300 days in ambient with three times enhancement in carrier mobility (0.015 $cm^2 \cdot V^{-1} \cdot s^{-1}$) compared to vacuum. This has been attributed to the enhanced polarization of hydroxyl groups in the presence of absorbed water molecules at the CuPc/PMMA interface. In addition, a model has been proposed based on the polarization of hydroxyl groups to explain the enhanced stability in these devices. We believe that this general method using a trilayer dielectric system can be extended to fabricate other OFETs with materials that are known to show high performances under vacuum but degrade under ambient conditions.



KEYWORDS: *dipole relaxation, anomalous bias stress, hysteresis, bilayer dielectric, organic field-effect transistor, stretched exponential function*

1. INTRODUCTION

Organic field-effect transistors (OFETs) have attracted immense attention in the last few decades due to their potential applications in transparent and flexible devices,[1] radio frequency identification (RFID) tags,[2] and chemical/biosensors.[3,4] However, the main challenges in OFET fabrication are their poor operational and environmental stability, which have been the subject of intense research in recent years.[5] The operational stability of these devices is typically represented by the stability under gate bias-stress and long time operation. In general, the drain current (I_{DS}) decays under gate bias-stress with time due to charge trapping into the traps present in the accumulation region.[6] In a few cases, the increase of I_{DS} was also observed under the bias-stress followed by normal decay. This has been explained in terms of slow polarization of gate dielectrics and was called the anomalous bias-stress effect in OFETs.[7,8] Such increase and decrease of I_{DS} under bias-stress crucially impacts the stability of the devices and requires minimization for the fabrication of efficient devices. The degradation of the devices under ambient conditions is another major impediment for the practical applications.[9] In such circumstances, the active semiconducting channel of the OFETs absorbs water molecules from ambient moisture. They act like charge carrier traps at the semiconductor−dielectric interface, resulting in poor carrier mobility and hysteresis in the transfer characteristics of the devices.[10−12] Water molecules can also be trapped within the dielectric layers by penetrating through the semiconductor layers.[13] In the presence of gate field, the trapped water molecules can be polarized and affects the device performance, resulting in a huge hysteresis in the transfer characteristics.[14] This is more pronounced for the devices operated under ambient conditions and fabricated with polymer dielectrics containing polar hydroxyl groups.[15] When the gate voltage is applied, the hydroxyl groups start polarizing slowly, since they are strongly attached with the polymer backbone. However, when water

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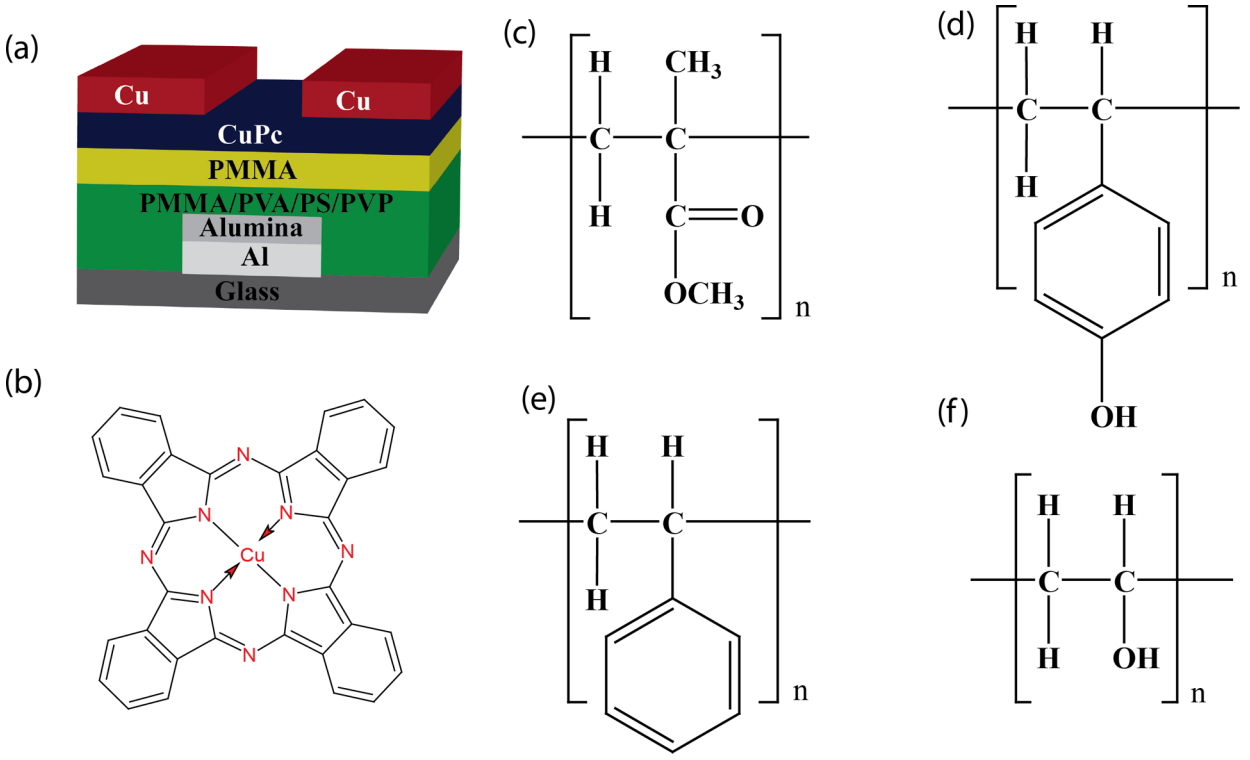

Figure 1. (a) Schematic diagram of the bottom-gate top-contact organic field effct transistor with polymer bilayer as the gate-dielectric. (b) CuPc, (c) PMMA, (d) PVP, (e) PS, and (f) PVA molecular structures.

molecules are absorbed, the hydroxyl groups easily attract polar water molecules and degrade the dielectric that reduces the stability of the devices.[16] Hence, the hydroxyl groups in the organic dielectrics play a crucial role in deciding the stability of the OFETs.[10] This has been an impending issue in the fabrication of stable OFETs, and crucial attempts have been reported in several literature reports to reduce the concentration of hydroxyl groups by cross-linking the polymer dielectric materials.[17,18]

The presence of hydroxyl groups in the dielectric layer has been reported to destabilize the performance of the devices due to adsorbed water molecules under ambient conditions.[19,20] Therefore, various research groups tried to reduce the density of the hydroxyl groups from the dielectric layers.[21,22] Nevertheless, it was also reported that the devices show huge hysteresis due to slow polarization of hydroxyl groups.[10,23] In this work, we report how the presence of hydroxyl groups in the dielectric layer can be exploited to enhance the carrier mobility and the stability of the devices. We have used a trilayer dielectric system consisting of a polar layer sandwiched between a hydrophobic polymer layer and a high-k inorganic layer. The reason for selecting an inorganic high-k dielectric layer is to reduce the leakage current and to optimize the thicknesses of the polymer dielectric layers used in the device. When the dielectric layer containing polar groups is separated from a semiconductor channel by a nonpolar dielectric, the adsorbed water molecules do not come into direct contact with the hydroxyl groups and remain at the interface of the semiconductor/hydrophobic dielectric layer. Under gate-field, these water molecules are also polarized and interact with the hydroxyl groups through the nonpolar layer. Additional charge accumulation was normally observed due to dipole polarization.[24] In this case, hydroxyl groups will be further polarized at a much faster rate than before, resulting in enhanced device stability with almost hysteresis free operation. In addition, the dielectric layer containing hydroxyl groups is protected from the possible degradation in the presence of water molecules. This further enhances the stability of the devices in the presence of ambient water molecules. In order to demonstrate this effect we have fabricated OFETs with CuPc as organic *p*-channel semiconductor materials, which are stable under ambient conditions. We have used PMMA, PVA, PVP, and polystyrene (PS) as dielectric materials, where PVA or PVP contain polar hydroxyl groups.[25,26] These layers were capped with a hydrophobic PMMA layer, which is used to eliminate the migration of water molecule into the buried polar dielectric layer.[27] On the other hand, PMMA and PS dielectrics do not contain any hydroxyl group. The devices with PMMA and PS as dielectrics are exhibiting hysteresis in ambient conditions due to the charge trapping by the water molecules.

2. EXPERIMENTAL SECTION

CuPc based OFETs with top contacts bottom gate configurations were fabricated by depositing a patterned 150 nm thick aluminum (Al) film on clean glass substrates used as gate electrode. A typical design of such devices is shown in Figure 1a. In order to reduce the leakage current and to minimize the thickness of the subsequent polymer dielectric layers, a 10 nm thick Al_2O_3 film was grown by converting a portion of Al film by an anodization process.[28−30] PVA (M_W = 89000−98000 g/mol), PS (M_W = 170000 g/mol), PVP (M_W = 25000 g/mol), CuPc (all Sigma-Aldrich) and PMMA (M_W = 5,50 000 g/mol) (Alfa-Aesar) were used without further purification. A set of polymer solutions were prepared by dissolving 30 mg/mL PVA in deionized water, 30 mg/mL PS in toluene, and 30 mg/mL PVP in freshly dried and distilled tetrahydrofuran (THF). Anodized substrates were spin coated by preprepared polymer

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solutions at 3000 rpm for 60 s and annealed at 100 °C for 1 h in a vacuum oven. The typical thickness of the individual polymer layer was about 70 nm. Subsequently, all the films were spin coated by about 30 nm thick PMMA films at 3000 rpm for 60 s and vacuum annealed at 100 °C for 1 h. We have fabricated four sets of devices containing a trilayer gate dielectrics system composed of PMMA (30 nm)/X(70 nm)/Al_2O_3(10 nm), with layer X indicating PMMA, PVA, PS, and PVP. These devices are named A, B, C, and D devices, respectively. In order to grow the active channel, a ∼60 nm thick CuPc film was deposited onto the polymer dielectrics under high vacuum conditions (<1 × 10^{-6} mbar) using a thermal evaporation technique with an optimized substrate temperature of 80 °C at a deposition rate of 0.02 nm/s. Finally, a 50 nm thick copper film was deposited onto the CuPc film as source and drain electrodes through a shadow mask, which defines the channel length (L) and channel width (W) as 25 and 750 μm, respectively. All capacitance−frequency (C−f) measurements, leakage current, current−voltage (I−V) characteristics, and bias-stress measurements of OFETs were carried out under vacuum (∼1 × 10^{-4} mbar) as well as under ambient conditions with 70% relative humidity (RH) using a Lake Shore probe station connected with a Keithley 4200 semiconductor characterization system (SCS).

3. RESULTS AND DISCUSSION

Figure1a shows the schematic diagram of the single and bilayer polymer dielectrics based OFETs with 10 nm alumina (Al_2O_3) employed in this study. Figure 1b−f shows the molecular structures of organic semiconductors and polymers used as active channel and dielectric materials. When the PMMA layer was used as the only dielectric layer to fabricate OFETs, the thickness of the layer was about 100 nm. However, when a bilayer polymer dielectric system was used, the thickness of PMMA was about 30 nm in combination with a 70 nm thickness either of a PVA or PVP or PS layer. The surface morphology of different dielectric layers of the dielectric system used for this study after the growth of an individual layer was studied using AFM. The typical AFM images of the surface morphologies of PMMA, PVA, PS, and PVP layers grown on an Al_2O_3 surface are shown in Figure S1, showing the surface roughness ranging within 0.12−1.22 nm. We observed the formation of pores of average size 120 nm in the PS films (Figure S1c). Further, a 30 nm thick PMMA layer grown on this layer not only made the surface smooth and pinhole free but also reduced the leakage current. Figure S2 in the Supporting Information shows the AFM images of PMMA deposited on other dielectric layers. The roughness of the PMMA layer deposited on PS and PVP was decreased to ∼0.4 nm, which is the highly smooth surface necessary for the growth of an organic channel. The leakage currents and capacitances of all the bilayer dielectric materials are shown in Figure S3. The use of a high-k inorganic dielectric layer (Al_2O_3) further reduced the leakage current. Figure S3a in the Supporting Information shows the typical leakage current density versus bias voltage plots of all dielectric systems. As can be easily seen from Figure S3a, bilayer PMMA/Al_2O_3 exhibits high leakage current (∼1 × 10^{-7} A/cm^2), whereas PMMA/PVA/Al_2O_3, PMMA/PS/Al_2O_3, and PMMA/PVP/Al_2O_3 trilayer dielectrics exhibit excellent insulating property, and their gate leakage current densities are on the order of only 10^{-8} A/cm^2. This reduction in leakage current can be attributed to the better quality of dielectric systems containing different dielectric constants.[31] The frequency dependencies of the capacitance density are shown in Figure S3b. The capacitance of the four dielectric materials was displayed in Table S1. PMMA and PMMA/PS dielectrics exhibit low capacitance compared to a PMMA/PVA device (57 nF/cm^2), because of the higher dielectric constant of the PVA (k = ∼9) compared to other dielectrics.

The performance of the OFETs crucially depends on the surface morphology of the active channel. Figure 2 shows the typical AFM images of the morphology of a 60 nm thick CuPc layer deposited on different dielectric surfaces with measured rms roughness in the range of 6.22−8.72 nm. We have observed the formation of dendritic like densely packed CuPc grains, and no uniform film formation is observed. Large grain boundaries affect the stability of the devices by absorbing different gases or water molecules from the moisture.[32] In order to study the stability of the devices under vacuum and ambient conditions, transfer characteristics and bias-stress measurements were performed on all the four devices. The effects of the measuring conditions on the performance and stability of the device in ambient and in a vacuum were investigated. Figure 3 shows the output characteristics (I_{DS} versus drain source voltage (V_{DS})) curves of the devices A, B, C, and D in vacuum, respectively. The devices show the p-type semiconducting behavior with clear linear and saturation behaviors below V_{DS} = −8 V, and the device can be operated within −12 V. Figure 4 shows the typical backward and forward transfer characteristic curves of devices A, B, C, and D measured under vacuum. The key device parameters, such as μ_{FE}, on/off current ratio (I_{on}/I_{off}) and threshold voltage (V_{Th}), were extracted using the equation of drain currents in the saturation region

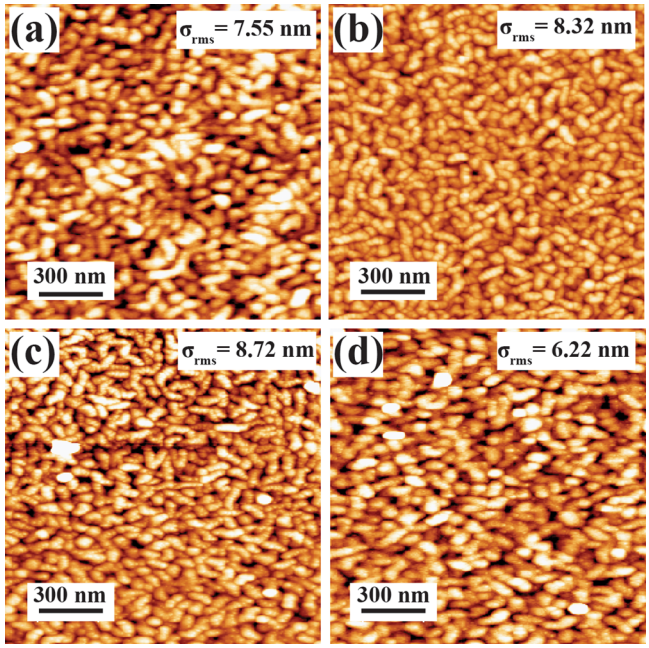

Figure 2. AFM topographic images of CuPc grown on (a) PMMA, (b) PVA/PMMA, (c) PS/PMMA, and (d) PVP/PMMA dielectric materials at 80 °C.

$$I_{DS} = \frac{\mu_{FE} C_{diel} W}{2L}(V_{GS} - V_{Th})^2 \quad (1)$$

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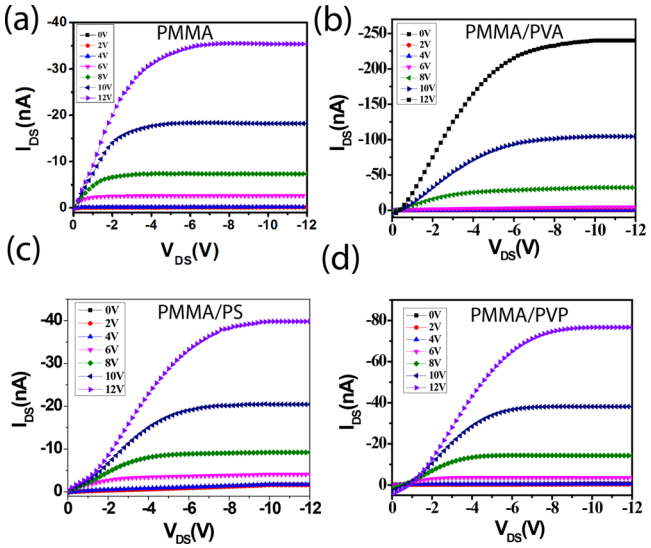

Figure 3. Output characteristics curves for the devices with PMMA(30 nm)/X(70 nm)/Al_2O_3(10 nm) as dielectrics in forward and backward scans. Here the X layer is indicating a layer containing (a) PMMA, (b) PVA, (c) PS, and (d) PVP. All the measurements were performed under vacuum.

where C_{diel} is the capacitance of the dielectric layer per unit area, and V_{GS} and V_{DS} are the gate-source voltage and drain-source voltage, respectively.[33] All the data listed are the average values of at least 10 devices on each of the samples, fabricated with common gate electrode and independent source drain electrodes. The transfer characteristics for devices A and C showed almost nil hysteresis as shown in Figure 4a and c. The corresponding threshold voltages for these two devices are −2.89 V and −3.02 V, respectively. On the other hand, devices B and D exhibit pronounced hysteresis with "ON to OFF" current higher than "OFF to ON" current, as shown in Figure 4b and d. It is noticeable that the devices with dielectric polymer possessing hydroxyl groups (B and D) produce higher hysteresis. In addition, as seen from Figure 4b and d, devices B and D exhibit a positive threshold voltage shift (ΔV_{Th}) of 0.93 and 0.81 V, respectively. Such behavior was also reported in the case of pentacene FETs with PVP−PMMA as dielectric system.[16]

To investigate the effect of moisture on the device performances, we measured the transfer characteristics of all the devices under ambient air with ∼70% RH. Figure 5 showed the transfer characteristics of all the four devices measured in ambient. Devices A and C showed noticeable hysteresis with "OFF to ON" current more than "ON to OFF" current, as shown in Figure 5a and c. These devices showed nil hysteresis when measured under vacuum conditions. The measured negative shifts in threshold voltage (ΔV_{Th}) in these devices are 0.11 and 0.29 V, respectively. Figure 5b and d showed the transfer curves for devices B and D. Interestingly, no hysteresis behavior was observed when measured under humidity conditions. However, these devices showed huge hysteresis under vacuum. Most notably, we also observed significant enhancement in carrier mobility in these devices when operated in ambient. All the device parameters are displayed in Table S2. We observed substantial enhancement in the performance of the devices under humidity conditions. In particular, device B showed more than three times mobility enhancement from 3.85 × 10^{-3} $cm^2/(V\ s)$ in vacuum to 1.2 × 10^{-2} $cm^2/(V\ s)$ under humidity conditions (Table S1 and S2). We estimated the average threshold voltages (V_{Th}) of the devices varying between −2.5 V and −5 V, subthreshold slope (SS) ranges 1.8−3 V/decade, and on off current ratio (I_{on}/I_{off}) of ∼10^3. These devices do not show any degradation in the performance even after exposing the device to ambient conditions for eight months. These results are in contrast to the earlier reports, in which the OFETs are reported to exhibit severe hysteresis under ambient conditions and display negligible hysteresis in vacuum.[34,35]

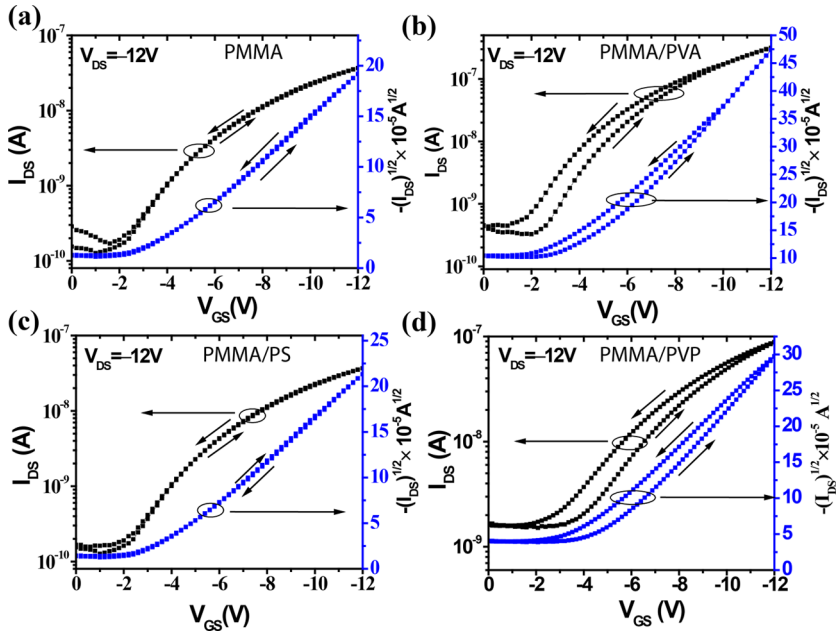

Figure 4. Transfer characteristic curves for the devices with PMMA(30 nm)/X(70 nm)/Al_2O_3(10 nm) as dielectrics in forward and backward scans. Here the X layer is indicating a layer containing (a) PMMA, (b) PVA, (c) PS, and (d) PVP. All the measurements were performed under vacuum.

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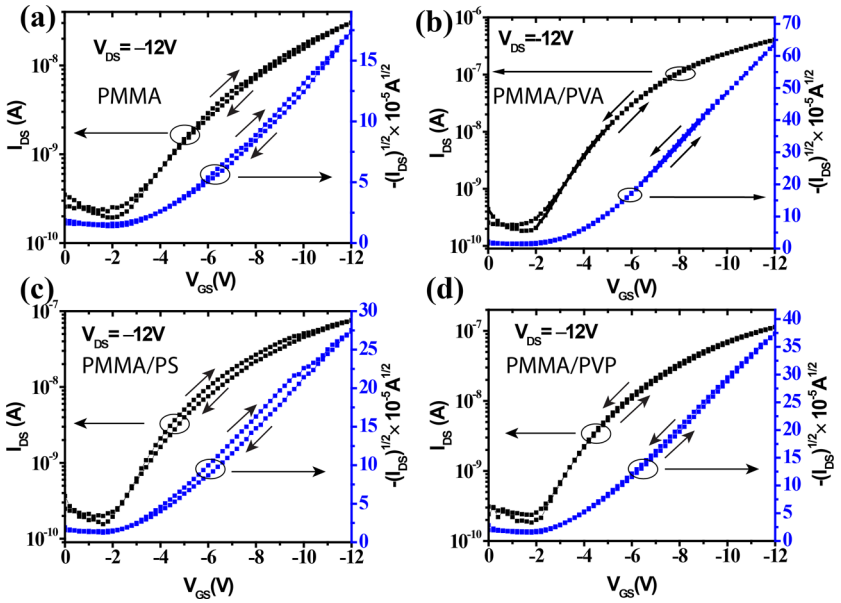

Figure 5. Transfer characteristics curves for the devices with PMMA(30 nm)/X(70 nm)/Al_2O_3(10 nm) dielectrics in forward and backward scans. Here the X layer is indicating a layer containing (a) PMMA, (b) PVA, (c) PS, and (d) PVP. Measurements were performed in ambient with 70% relative humidity.

Current decreases during backward sweep (ON to OFF) are often attributed to the charge carrier trapping at the interface.[36] However, an increase in the ON to OFF current observed in devices B and D in vacuum could be due to any one of the following three mechanisms: (1) charge injection from the gate electrode, (2) mobile ions in the dielectric, or (3) the slow polarization of dipoles present in the of polymer dielectric.[37,38] The possibility of charge injection from the gate into the channel is very poor in the case of a trilayer dielectric system including high *k*-materials which we used for the fabrication of these devices. Nevertheless, we have observed similar results for the devices fabricated with Si++/SiO_2(300 nm)/PVA/PMMA (Figure S4), where the possibility of charge injection from the gate into the channel would be negligible due to a very high quality and thick SiO_2 layer. Mechanism 2 can also be eliminated because both PVA and PVP dielectrics are capped with a 30 nm thick PMMA layer, which can block the diffusion of ions into the interface of CuPc/PMMA. Hence, polarization of hydroxyl groups is possibly the origin of the hysteresis observed in these devices. The hydroxyl groups in the polymer dielectric material act like electron traps. When they are at the interface of a dielectric/organic semiconductor, the performance of the devices degraded under long-term operation. In that case, the hydroxyl groups try to orient slowly in the direction of the field generated by the applied gate voltage. In our case the slow polarization of dipoles (Mechanism 3) due to a gate electric field could be responsible for the observed hysteresis effect in devices B and D measured under vacuum. Similar observations are also reported in the case of OFETs based on pentacene with PVP as gate dielectric layer.[39] The adsorbed water molecules significantly influence the slow polarization of the hydroxyl groups when the polar dielectric layer is capped with a hydrophobic layer.

In order to understand the effect of the concentration of water molecules at the interface, we have studied the performance of the B device in 40% and 100% RH, in addition to 70% RH. Figure 6 shows the transfer characteristic curves measured under the above two humidity conditions. We have

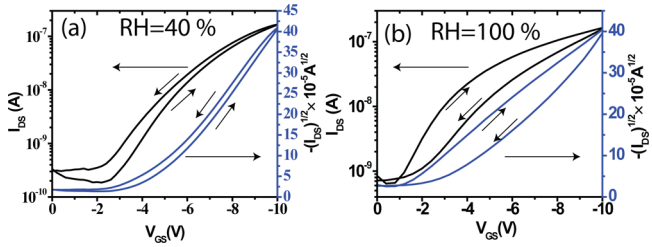

Figure 6. Dual sweep transfer characteristics of the CuPc/ PMMA/ PVA/Al_2O_3/Al device (B device) under (a) RH = 40% and (b) RH = 100% at V_{DS} = −7 V.

observed the reduction in hysteresis at 40% in comparison to the value measured under vacuum. In addition, the ON to OFF current is still higher than the OFF to ON current. The measured hysteresis becomes almost nil at 70% RH, as shown in Figure 5b. We observed a further increase in hysteresis at 100% RH. However, in this case, the OFF to ON current was found to be higher than the ON to OFF current at 100% RH. As we increased the relative humidity, the concentration of water molecules at the interface of the CuPc and PMMA layers increased. The effect of water molecules in the polarization of the dielectric layer can be explained in terms of the local field produced by the external field and the field produced by the individual dipoles. In that case, the depolarizing field, which acts against the applied gate field, can be written as $\vec{E}_1 = -\vec{P}/\varepsilon_0$, where $\vec{P}$ is the average polarization vector. This field diminishes the applied external gate field ($\vec{E}$) within the layer. However, the local field ($\vec{E}_{local}$) experienced by the individual dipoles within the dielectric layer can be written as $\vec{E}_{local} = \vec{E} + \vec{P}/3\varepsilon_0$.[40] This field is greater than the applied gate field. Therefore, individual dipoles experience greater force locally, which helps them to be further polarized. In addition, water molecules are also polar molecules and get polarized under the gate field. The local dipole field due to the polarization of water molecules enhances the polarization of the hydroxyl groups further. We believe that as a result of enhanced polarization of hydroxyl

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groups in the presence of water molecules, the dielectric constant of the materials enhanced. The capacitance−voltage (CV) measurements carried out on the dielectric systems used in this work indeed show the systematic increase of capacitance of the dielectric system with the concentration of water molecules (see Figure 7). In fact, the Clausius−Mossotti

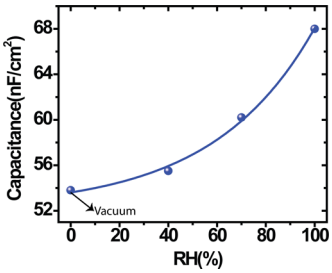

Figure 7. Variation of the effective capacitance of the PMMA/PVA/Al_2O_3 dielectric system with the variation of relative humidity.

relation for predicting the dielectric constant of a dielectric material also confirms the enhancement of the dielectric constant with the dipole polarization.[40] Therefore, the polarization of hydroxyl groups is enhanced at a much faster rate in the presence of water molecules at the interface. As a result, the hysteresis decreases with humidity and is completely canceled at 70% RH. At this humidity condition the adsorbed water molecules fill the interface, forming a water layer, and the total dipole moment of the water molecule is sufficient enough to saturate the polarization of hydroxyl groups. Therefore, at humidity condition beyond 70% RH, the additional adsorbed water molecules cannot reach the interface any more, since water molecules already saturate the interface at 70% RH. As a result, the additional water molecules beyond 70% RH act like traps at the semiconductor layer. The observation of higher OFF to ON current than ON to OFF current is the signature of the trap induced effect.[36]

On the other hand, in the absence of a capping layer in the dielectric system, the polar dielectric layer is exposed to a semiconductor channel and the adsorbed water molecules directly interact with the polar hydroxyl groups. Therefore, the polarization of the hydroxyl groups as a result of applied gate voltage minimizes and destabilizes the performance of the devices. In the presence of a capped layer, the field induced by the polarized hydroxyl groups diminishes the applied gate bias. However, the total capacitance of the dielectric systems under these conditions increases as depicted in Figure 7, showing the variation of capacitance with relative humidity. This confirms that the dielectric constant defined by $C = (k\varepsilon_0 A)/d$, with k dielectric constant, $\varepsilon_0$permittivity, A cross-sectional area, and d thickness of the dielectric system, increases with humidity. If we consider that the total thickness of the dielectric system is not changed due to the presence of the adsorbed water at the interfaces of semiconductor/PMMA, then the enhanced dielectric constants can be attributed to the enhanced polarization of hydroxyl groups due to the adsorbed water molecules.

In order to understand the origin of the enhanced stability of these devices under ambient conditions, we have investigated the bias-stress measurements on these devices in vacuum as well as under ambient conditions. There are several reports which demonstrated that the moisture is the main cause of bias-stress instability and the hysteresis in OFETs containing polymer dielectrics. This is more severe when the polymer contains polar groups, which capture water molecules and degrade the dielectric properties of the polymers. Our results show enhanced stability with hysteresis free operation in the presence of water molecules. Figure 8a and b shows the time

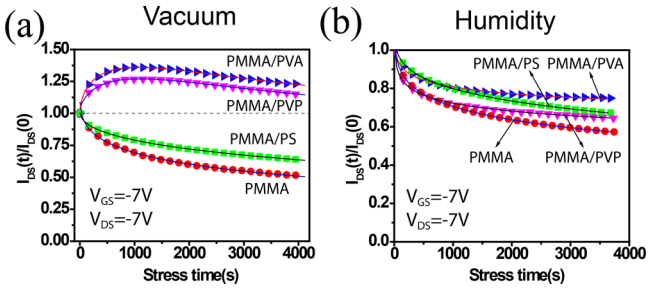

Figure 8. (a) Temporal evolution of normalized I_{DS} under bias-stress in vacuum. (b) Temporal evolution of normalized I_{DS} under bias-stress in 70% relative humidity. In (a) and (b) the solid symbols indicate the experimental data and continuous solid lines indicate the fitting curve.

dependent variation of I_{DS} under constant bias-stress (V_{GS} = V_{DS} = −7 V) for about 1 h in vacuum and under humidity conditions, respectively. In vacuum, devices B and D show anomalous behavior with an increase in current by about 30−40% initially followed by decay. On the other hand, devices A and C exhibited the usual I_{DS} decay profile under 1 h of bias-stress. The decay in I_{DS} during electrical bias-stress is commonly related to the charge carrier trapping at the interface of the dielectric and organic semiconductors channel, or within the bulk of the semiconductor.

The normal I_{DS} decay can be expressed with a stretched exponential function as[41,42]

$$I_{DS}(t) = I_0(0)\exp\left[-\left(\frac{t}{\tau_d}\right)^{\beta}\right] \quad (2)$$

where $I_0(0)$ is the drain current at time $t = 0$, β is the dispersion parameter whose value belongs within $0 < \beta < 1$, and τ_d is the characteristic decay time. The solid lines shown in Figure 8a are the typical fitting of I_{DS} for devices A and C using the above equation. The fitting parameters are summarized in Table 1. The values of β obtained from the fitting for devices A and C are 0.37 and 0.45, and the values of τ_d for the same devices are 3.9×10^3 s and 2.1×10^4 s, respectively. It is noticeable that, in both cases, the β values do not change significantly but τ_d increased enormously for the device C. This indicates that the devices fabricated with trilayer PMMA/PS/Al_2O_3 dielectric can effectively reduce the interface traps and increase the decay time by 1 order of magnitude higher than the devices fabricated with bilayer PMMA/Al_2O_3. In case of devices B and D, the current initially increased until a certain time and then decayed under bias-stress following a normal decay profile. This observation of anomalous bias-stress effect under vacuum can be attributed to the slow polarization of the dipoles present in the polymer dielectric under applied bias-stress. In the case of polar polymer dielectrics, the permanent dipoles (i.e.,−OH groups) are strongly attached to the backbone of the polymer with an orientation perpendicular or parallel to the main chain.[43] These dipoles will orient slowly under the applied electric field with a relaxation time in the range of seconds to days. Thus, it is expected that the polar counterparts of the

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Table 1. Summary of Fitted Parameters in Vacuum and Ambient Conditions Using the Stretched Exponential Functions: α and β are Dispersion Parameters, τ_p and τ_d Are the Characteristic Times for the Polarization and Trapping

		α	β		τ_p (s)	τ_d (s)	
Device	Name of the dielectric	*Vacuum*	*Vacuum*	*Ambient*	*Vacuum*	*Vacuum*	*Ambient*
A	PMMA		0.37	0.28		3900	4471
C	PMMA/PS		0.45	0.33		21000	16965
B	PMMA/PVA	0.69	0.75	0.14	670	2400	868
D	PMMA/PVP	0.74	0.71	0.16	1400	2700	546

polymer, i.e., −OH, groups in the PVA and PVP are slowly polarized under gate bias. As the polarization increases with time, the aligned dipoles induce additional charges in the accumulation region. Therefore, we observed an enhancement of drain current up to a certain time, until which the polarization of the dipoles saturates. The time required to reach the maximum current depends on the value of the polarization time constant (τ_p) for the particular dielectric material. However, the current decays due to the traps, as observed in the case of devices A and C in vacuum, did not show any anomalous effect. Therefore, the induction of additional holes into the interface due to polarization of hydroxyl groups and the charge trapping at dielectric/semiconductor interfaces are the two competing phenomenon occurring at the same time. As a result, the anomalous behavior observed under bias-stress for devices B and D cannot be simply explained by stretched exponential function alone. It is necessary to include the orientation of dipoles with respect to the time under the continuous gate bias, while calculating I_{DS}. Hence, we modified the traditional stretched exponential function used for I_{DS} decay by introducing the polarization term. The additional induced current due to the polarization of the dipoles can be considered as[44,45]

$$I_{DS}(t) = I_0(0)\left\{1 - \exp\left[-\left(\frac{t}{\tau_p}\right)^{\alpha}\right]\right\} \quad (3)$$

Dipole orientation and charge trapping are the two independent phenomena. Therefore, the effective drain current can be expressed as

$$I_{DS}(t) = I_0(0)\left[\left\{1 - \exp\left[-\left(\frac{t}{\tau_p}\right)^{\alpha}\right]\right\} + \exp\left[-\left(\frac{t}{\tau_d}\right)^{\beta}\right]\right] \quad (4)$$

where α and β represent the dispersion parameters describing the distribution of activation energy for the charge inducing in the active channel and charge trapping in the interface and channel. Here, τ_p and τ_d represent the characteristic time constants for charge induction due to polarization and charge trapping, respectively. We used eq 4 for the fitting of anomalous behavior of drain current for devices B and D. Interestingly, all the devices showed normal I_{DS} decay as depicted in Figure 8b in humidity conditions. The shapes of the curves indicated that the rapid I_{DS} decay in B and D devices in the early stages compared to A and C devices most likely originated from charge trapping at the interface due to the absorbed water molecules from the atmosphere. We used eq 2 for the fitting of the I_{DS} decay curves measured in ambient. The corresponding fitting parameters are displayed in Table 1. Higher τ_d observed for the case of PMMA/PS/Al_2O_3 dielectric essentially represents lower trap density. In general, the value of this parameter decreases under ambient conditions. This represents the increase in traps due to the absorption of water molecules. The absorption of water molecules is more in the case of polar dielectric materials than nonpolar ones. The value of τ_p for device B is less than that of device D in vacuum. This indicates that the polarization in the dielectric is slow in device D fabricated with PVP. The initial decay in a stretched-exponential formula is strongly coupled to the β value, such that smaller β value yields more rapid decays, during the early stages of a current decay. We observed that the β value was decreased in ambient compared to vacuum in all the devices. Particularly, the β value was decreased significantly in ambient in devices B and D. Here α represents the distribution of the activation energy for polarization (ΔE_α), following the relation, $\Delta E_\alpha = k_B T/\alpha$, and β represents the distribution of the activation energy for charge trapping (ΔE_β), following the relation, $\Delta E_\beta = k_B T/\beta$, where k_B is the Boltzmann constant and T is the absolute temperature. All the parameters for the distribution of activation energies are tabulated in Table 2. We

Table 2. Summary of Activation Energies for Charge Trapping and Dipole Polarization in Vacuum and Ambient Conditions

	$\Delta E_\alpha = k_B T/\alpha$ (eV)	$\Delta E_\beta = k_B T/\beta$ (eV)	
Device	Vacuum	Vacuum	Ambient
A		0.069	0.092
C		0.057	0.078
B	0.037	0.034	0.183
D	0.035	0.036	0.161

observed a wider distribution for the activation energy for charge trapping in ambient compared to vacuum. This indicates that the mean barrier height for the charge trapping was increased in the presence of water molecules. The ΔE_β value was increased in ambient conditions compared to vacuum. Particularly in B and D devices, this value was increased by more than five times. The energies of the trap sites are strongly affected by the absorbed molecules, and this absorption depends on the nature of the dielectric material. Here, B and D devices contain hydroxyl groups in the inner dielectric material, which can readily interact with the water molecules absorbed from the ambient and influence the interface trap energies.[46] We observed that the activation energies for polarization (ΔE_α) and charge trapping (ΔE_β) are nearly equal in vacuum as shown in Table 2.

In order to confirm that the observed effect is purely the intrinsic behavior of dielectric system, we have fabricated another set of devices with a PTCDI-Br_2-C_{18} molecule as channel material, which shows n-type behavior.[30] The structure of the molecule and the schematic diagram of the device are shown in Figure S5. We have observed similar anomalous effects in hysteresis and bias-stress measurements as shown in

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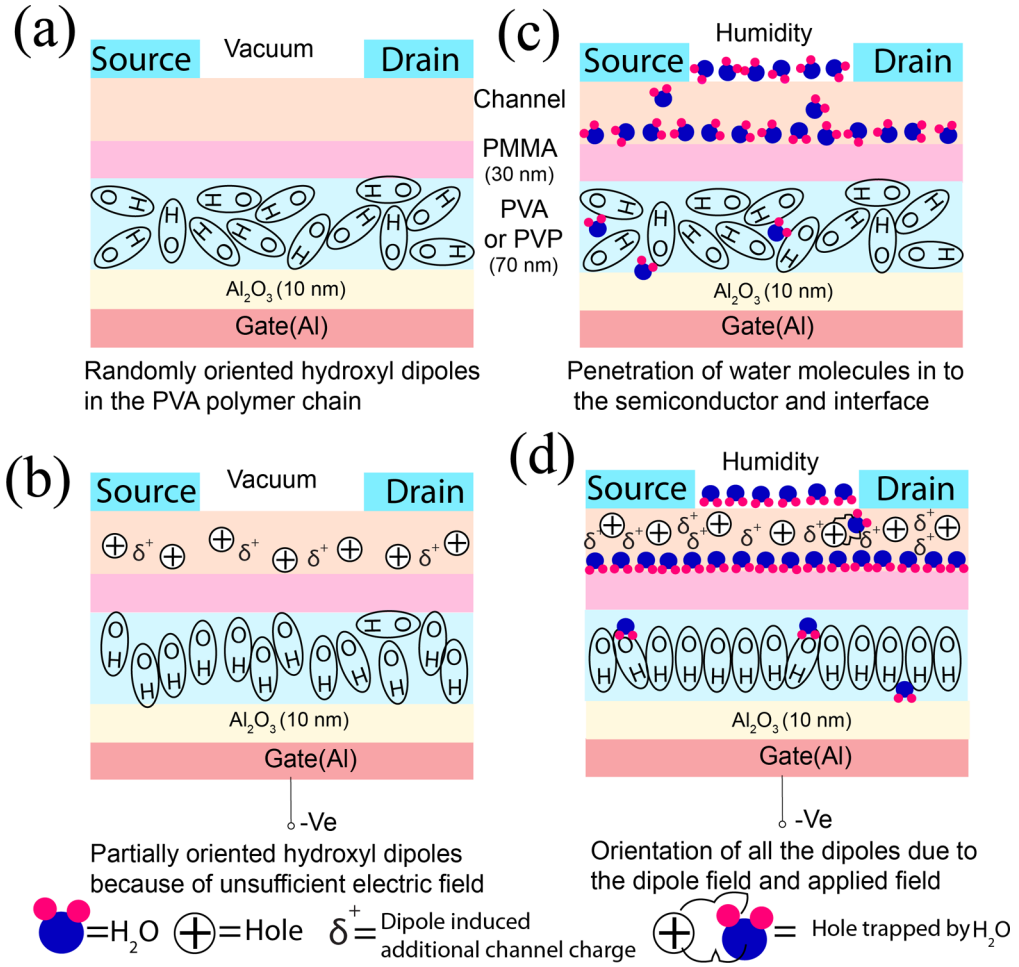

Figure 9. (a) Schematic illustration of randomly oriented OH groups in the polar dielectric layer. (b) Partially oriented −OH groups due to applied gate voltage in vacuum. (c) Randomly oriented −OH groups with absorbed water molecules. (d) Fully oriented −OH groups due to applied gate voltage in 70% relative humidity and high dipole moment of the water dipole layer.

Figure S6. This confirms that our observations do not depend much on the organic semiconductor materials used for the fabrication of the devices. The dependency of observed hysteresis on the type of bias and the magnitude of bias are essentially due to the effect of polarization of the dipolar dielectric layer in the presence of gate field. Such effects are generally observed on the OFETs fabricated with a dipolar dielectric layer.

Finally, we propose a model in order to understand the behavior of hysteresis and bias-stress in vacuum and humidity conditions. The model is schematically illustrated in Figure 9. The proposed model describes the polarization of hydroxyl groups and their interactions with absorbed water molecules. Under vacuum, no water molecules are present in the devices and the hydroxyl groups are randomly oriented within the PVA or PVP layer with no bias condition, as shown in Figure 9a. When the gate bias is switched on, the hydroxyl groups begin to orient (see Figure 9b) along the gate-field direction and the maximum polarization occurs at time τ_p. During the process of dipoles getting aligned along the gate field, they keep inducing additional charges in the accumulation layer. As a result, we observed the increase in the drain current, as shown in Figure 8a. When the devices were exposed to normal ambient conditions with 70% RH, water molecules were absorbed and distributed on the semiconductor as well as in the channel, as shown in Figure 9c. As the polar dielectric layer was capped with the PMMA layer, which is hydrophobic in nature, the adsorbed water molecules could not diffuse into the PVA or PVP layer and form a layer of water molecules at the interface. However, few water molecules may permeate through the pores of PMMA and reach the polar dielectric, but most of them are expected to remain at the surface and the interface, forming a water dipole layer.[12]

When the gate voltage is switched on, the hydroxyl groups begin to polarize as before. Since the water molecules also possess permanent dipole moment, all the water dipoles present at the interfaces are also polarized immediately and caused a huge dipole moment at the interface. This dipole field interacts with the polar hydroxyl groups through the nonpolar 30 nm thick PMMA layer. As a result, the hydroxyl groups are polarized much faster in the presence of water as compared to vacuum conditions where there were no water molecules in the devices. Therefore, the induced charges at the accumulation layer are further enhanced, eliminating the anomalous effects arising due to the slow polarization in the absence of water molecules. This further enhanced the drain current. The observed maximum increase in drain current is from 218 nA to 422 nA, during the environmental conditions changed from vacuum to ambient in the case of device B. The mechanism of polarization of hydroxyl groups in the presence of water molecules is schematically illustrated in Figure 9.

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4. CONCLUSIONS

In summary, we have demonstrated the enhanced performance with higher operational and environmental stabilities of CuPc based OFETs, when a polar dielectric layer is capped with a hydrophobic dielectric layer. The improved performances of the devices have been attributed to the fast polarization of hydroxyl groups by the polarized adsorbed water molecules at the interface. The observed hysteresis and anomalous bias-stress in vacuum was explained by the slow polarization of the bulk dipoles under the gate field. In addition, while quantitatively analyzing the anomalous bias-stress observed in the absence of water molecules, we have introduced the effect of polarization hydroxyl groups into the stretched exponential decay of the drain current. We proposed a model to understand the mechanism based on the observed results. Therefore, contrary to the existing notion that organic devices generally degrade at ambient conditions, we have developed a new concept of stabilizing and enhancing the performance of CuPc based OFETs with PVA or PVP as one of the dielectric layers. These devices not only exhibited high environmental stability with hysteresis-free performances but also showed remarkable improvement in several other device parameters, such as carrier mobility and their long-term stability.

■ ASSOCIATED CONTENT

Supporting Information

AFM topography images of inner dielectric layers of PMMA, PVA, PS, and PVP. AFM images of PMMA layer coated as second layer, and images of capacitance and leakage current. Schematic illustration of SiO_2/ PVA/PMMA/CuPc device structure and transfer characteristic curves are presented. Device properties of PTCDI-Br_2−C_{18} based OFETs. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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